JONATHAN HUANG

jonrhuang@gmail.com | 908-249-3341 | linkedin.com/in/jonathan-ray-huang

TECHNICAL SKILLS

Languages: C, C++, Rust, Bash, Python, Perl, System Verilog, Verilog, Assembly, Matlab
Technology/Tools: Linux, Git, Jira, Agile methodology, Xilinx Vivado, Cadence Virtuoso, Questasim, AWS, Docker, Gem5, FPGA, Verilator

WORK EXPERIENCE

BROWN DEER TECHNOLOGY – BEL AIR, MARYLAND June 2024 – Present
Computer Hardware Engineer

- Testing and verifying functionality of existing four-stage and five-stage 32-bit RISC-V soft processor cores
- Developing RISC-V extension components, instruction cache, and data cache for 32-bit and 64-bit RISC-V processor in Verilog
- Maintaining and developing test packages for multiple processors using assembly, C, and bash
- Creating bash scripts and tools to streamline development workflow
- Researching potential use cases and additional features for the soft processor cores
- Programming FPGAs with basic test functionalities using Xilinx Vivado
- Providing mentorship to intern, focusing on programming skills in C to create unique test cases

PURDUE UNIVERSITY – WEST LAFAYETTE, INDIANA August 2023 – May 2024
Student Researcher

- Simulated the team's RISC-V core using Gem5.
- Utilized Embench test suites to monitor performance and guide architectural improvements.
- Led architecture development of the cache and ram using Gem5 to enhance memory performance by 15% through configuration optimizations

IEEE – PISCATAWAY, New Jersey May 2023 – August 2023
Cloud Engineer

- Researched ways to increase observability of resource usage on AWS EKS.
- Created a comprehensive run book outlining set up instructions for integrating Open Telemetry, Prometheus, and Grafana, ensuring streamlined implementation across current and future applications
- Wrote a lambda function to increase observability within AWS Batch jobs.

IEEE – PISCATAWAY, New Jersey May 2022 – August 2022
Software Engineer

- Identified over 15 major and recurring issues with applications or processes by implementing new data science clustering and NLP techniques in Python to process help desk tickets.
- Communicated with the business relations team, database team, and infrastructure team to collect and organize application and licensing data for the migration to a new data storage software.

PROJECTS

Multicore Processor System Verilog, Questasim, Git | May 2023

- Prototyped processor with a five-stage pipeline, two-way set-associative data cache, direct mapped instruction cache, along with MSI cache coherence protocol for dual-multicore.
- Achieved synchronization support with LL-SC in the data path, along with parallel programs in MIPS assembly.
- Verified components and final integration of design using System Verilog testbenches and the comparison of memory traces with various self-written MIPS test cases.